

1 ABSTRACT

2 A high speed communications interface divides data into a
3 plurality of lanes, each lane encoded with clocking
4 information, serialized, and sent to an interface. During
5 cycles when there is no available data to send, IDLE_EVEN
6 and IDLE_ODD cells are sent on alternating cycles. Data is
7 transmitted by sending a header which spans all lanes and
8 includes a START symbol. The final data transaction
9 includes a Frame Check Sequence (FCS) which operates over
10 the entire header and data. The packet is terminated by an
11 END symbol, which is sent after the final data, and the
12 remainder of the lanes are padded with IDLE_EVEN, IDLE_ODD,
13 IDLE_EVEN_BUSY, or IDLE_ODD_BUSY cycles. The interface has
14 a variable clock rate.